Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	7462	fabricat$3 same wafer same transistor	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:34
L10	300	(fabricat$3 same wafer same transistor) same (location)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 12:45
L11	68	10 and lithograph$4	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:37
L12	12	11 and (interconnect same metal)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 12:46
L13	12	12 and substrate	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 12:47
L14	8	13 and (test$3 or check$3 or verification or evaluation)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 12:47
L15	8	14 and (level or layer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 12:48
L16	2126	fabricat$3 same wafer same transistor and test$3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:34
L17	396	fabricat$3 same wafer same transistor same (test$3 or check$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:35
L18	130	17 and ((interconnect or (metal adj layer)) same (test$3 or check$3))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:36
L19	81	17 and ((interconnect or (metal adj layer)) with (test$3 or check$3))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:36
L20	14	19 and (lithograph$4 same fabricate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 13:37

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1311	(test$4 or check$3 or verification or evaluation) same (wafer with (transistor or circuit)) same (location or position)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 09:21
S2	533	(test$4 or check$3 or verification or evaluation) same (wafer with (transistor or circuit)) same (paramet$5)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:31
S3	2	(test$4 or check$3 or verification or evaluation) same (wafer with (transistor or circuit)) same ((connect$3 or hook-up or hook or attach$5) with (lithographic or litho-grahic))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:33
S4	1	S1 and S2 and S3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:33
S5	138	S1 and S2	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:33
S6	17	S5 and (lithographic or litho-grahic)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:45
S7	29	S5 and (lithographic or litho-grahic or photolithographic or photolitho-grahic)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:49
S8	29	S7 and (subset or sub-set or set)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 17:56
S9	24	S8 and (conductor or interconnect$4 or metal) and level	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 18:13
S10	12	S9 and (vector same test)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 18:13
S11	26	S8 and (conductor or interconnect$4 or metal) and (level or layer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 18:13
S12	15	S8 and (conductor or interconnect$4 or metal) adj (level or layer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 18:14
S13	8	S12 and (test same vector)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 18:21
S14	8	S13 and (test same structure)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/24 18:21

S15	237	(test$4 or check$3 or verification or evaluation) same (wafer with (transistor or circuit)) same (location or position) same fabricat$3	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 09:22
S16	130451	(test$4 or check$3 or verification or evaluation) same (parameter)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 09:22
S17	83	S15 and S16	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 09:22
S18	35	S17 and (lithograph$4 or litho-graph$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 09:23
S19	35	S18 and (subset or sub-set or set)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/08/26 12:44